

STAGGERED PULSE ACQUISITION METHOD AND APPARATUS

CROSS REFERENCE TO RELATED APPLICATION

This application claims priority from U.S. Provisional Patent Application Serial No. 60/253,131, entitled "Staggered Pulse Acquisition Method and Apparatus," filed November 28, 2000. The disclosure of that provisional patent application is incorporated by reference here in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to data communication systems and, more particularly, to data communication systems transmitting and receiving signals in the presence of unintentional background noise or intentional interference.

Description of the Related Art

The ability to detect and acquire low level communications, navigation, or radar signals in the presence of unintentional background noise or intentional interference (jamming) has been and continues to be a critical requirement for numerous military and civilian systems.

Traditional solutions include increasing the transmitted signal power, sometimes adaptively, to allow operation with various levels of interference. One such application is for the next generation of the Global Positioning System (GPS). The military community requires additional anti-jam (A/J) capability for the GPS military signal in theaters or areas of responsibility (AORs) during times of conflict. One proposal that has been submitted to achieve this capability is to configure the GPS satellites with large, steerable dish antennas that can direct high power spot beams into an AOR.

Another solution, for synchronous communications systems, is to increase the signal power in short bursts with duty cycles that are of the order of the reciprocal of the power increase. With this scheme, the average power is not increased and, since the system is

1 synchronous, the receiver can anticipate when the bursts, or pulses, will occur. If the receiver
2 is only trying to acquire the signal during the occurrence of a pulse (or pulses), then the
3 resistance to interference is improved by the amount of the instantaneous power increase.

4 However, the brute force technique of raising the average power to counteract
5 interference or jamming generally is expensive and is limited by the power resources
6 available at the transmitter. The proposal to increase power in a selected geographical area
7 via spot beams for the next generation of GPS is extremely expensive, in terms of cost,
8 operational complexity, and size, weight and power of the required satellite equipment.

9 The pulsed power technique discussed above is an elegant solution, but it requires
10 synchronous operation. The receiver must have its internal clock synchronized with the
11 transmitter's clock, in order to be able to anticipate the occurrence of the high power signal
12 pulses. If the receiver cannot predict when the pulses will occur, then the receiver will
13 continuously attempt to acquire the signal. Accordingly, no advantage will be realized from
14 the pulsing technique, because the total signal energy in the receiver's acquisition window
15 will be the same as without pulsing. Also, if the power is pulsed at a regular rate, a jammer
16 can pulse the jamming power at nearly the same rate so that periodically the jamming pulses
17 will synchronize with the signal pulses at the receiver, giving an advantage to the jammer to
18 at least periodically block the signal.

19 Accordingly, there is a need for a system that increases the signal power in short
20 bursts but that does not require synchronous operation.

21 SUMMARY OF THE INVENTION

22 Therefore, in light of the above, and for other reasons that will become apparent when
23 the invention is fully described, an object of the present invention is to extend the pulsed
24 power technique to non-synchronous systems.

25 Another object is to reduce the power requirements of a transmitter, such as a
26 transmitter in a GPS satellite that transmits a signal such as a GPS signal.

27 Still another object is to avoid the need to configure satellites transmitting the signal
28 with steerable antennas.

1 The aforesaid objects are achieved individually and in combination, and it is not
2 intended that the invention be construed as requiring two or more of the objects to be
3 combined unless expressly required by the claims attached hereto.

4 In accordance with the certain aspects of the invention, high power pulses are
5 staggered in time such that the length of the time intervals between pulses are known to the
6 receiver, so that the receiver can utilize this knowledge to reliably acquire the signal, without
7 time synchronization. The duration of the time intervals between the high power pulses can
8 be cryptographically controlled using a cryptographic key known to both the transmitter and
9 the receiver, so that authorized receivers are given an advantage.

10 The acquisition strategy for the receiver is to configure the correlators to detect only
11 the high-power portions of the code, ignoring the low-power portions. The tracking strategy
12 is to switch the gain level to follow the anticipated power profile, providing separate
13 weighting of the two components of the received signal. (In a typical receiver, the
14 acquisition mode allows the receiver to discover the correct signal timing, and the tracking
15 mode allows the receiver to follow any drift of the timing.)

16 The rationale for this strategy is as follows. The tracking portion of a receiver
17 typically needs only a few correlators (generally with on-time, early, and late phases); so that
18 giving some weight even to the low-power portions of the signal can be afforded. However,
19 the acquisition portion of the receiver typically needs as many parallel correlators as can be
20 afforded, to allow searching for the correct timing as quickly as possible. Giving zero weight
21 to (ignoring) the low-power portions of the signal (as illustrated by the bottom half of Fig. 2)
22 reduces the amount of processing, allowing more correlators for the same cost.

23 The above and still further objects, features and advantages of the invention will
24 become apparent upon consideration of the following descriptions and descriptive figures of
25 specific embodiments thereof. While these descriptions go into specific details of the
26 invention, it should be understood that variations may and do exist and would be apparent to
27 those skilled in the art based on the descriptions herein.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a conventional received signal and operation of a conventional correlation receiver.

Fig. 2 shows a staggered pulse signal according to aspects of the present invention and operation of a receiver used to acquire the staggered pulse signal.

Figs. 3A and B are block diagrams of exemplary transmitters having an amplifier that boosts certain chips of a pseudonoise (PN) code according to a cryptographic algorithm and outputs a sequence of staggered high-power chips forming a power pulse.

Fig. 4A is a block diagram of an exemplary receiver configured to operate in a tracking mode to track the staggered high-power chips output from the transmitter.

Fig. 4B is a block diagram of another exemplary receiver configured operate in an acquisition mode to receive and acquire code having the staggered high-power chips output from the transmitter.

Fig. 5A is a block diagram of a matched-filter style of coherent correlator, correlating over one power pulse.

Fig. 5B is a block diagram of a parallel-active style of coherent correlator, correlating over one power pulse.

Fig. 6A shows a matched-filter style of a partially coherent correlator which can correlate multiple power pulses. The correlator in Fig. 6A employs a series of the matched-filter style coherent correlators shown in Fig. 5A.

Fig. 6B shows an active-parallel style of a partially coherent correlator which can correlate multiple power pulses. The correlator in Fig. 6B employs a series of the parallel-active style coherent correlators shown in Fig. 5B.

DETAILED DESCRIPTION

Preferred embodiments according to the present invention are described below with reference to the above drawings, in which like reference numerals designate like components.

Operation

To achieve the advantages of using high-powered pulses without requiring a receiver to operate non-synchronously with a transmitter, a new signal has been developed. In that

1 new signal, groups of high-power pulses are staggered in time such that the duration of time
2 intervals between the groups of pulses vary and are known to the receiver. This allows the
3 receiver to utilize that knowledge to reliably acquire the signal, without time synchronization.
4 The length of the time intervals between the groups of high power pulses can be
5 cryptographically controlled using a cryptographic key known to both the transmitter and the
6 receiver.

7 For a code division multiple access (CDMA) signal structure, a conventional
8 correlation receiver operates as depicted in Fig. 1. A 45-chip segment of a code 1 that the
9 receiver attempts to acquire is shown in Fig.1. The code (chip sequence) is stored in the
10 receiver, usually 2 samples per chip, shown in Fig. 1 as code 2. The receiver compares the
11 received signal with the stored code 2. The comparison can be accomplished by correlating
12 the received signal with the stored code 2 by taking the dot product of the stored sequence
13 with a corresponding length of incoming signal. Then, on every succeeding time sample ($\frac{1}{2}$
14 chip), the incoming signal is shifted by one sample and a new dot product is formed. When
15 the shifted incoming signal aligns (within $\frac{1}{2}$ chip) with the stored code 2, the output of the
16 correlator, that is, the value of the dot product, will be much higher than at other times. The
17 amount by which the correlation peak exceeds the non-peak values depends on the length of
18 the correlator and on the correlation properties of the particular code that is being used. The
19 signal is deemed acquired when the correlator output exceeds a pre-determined threshold.

20 To illustrate the operation of pulse acquisition according to an aspect of the present
21 invention, consider the same code sequence that was utilized in the above example, with the
22 signal power boosted for short intervals creating pulses that include a plurality of chips with a
23 boosted signal power, as depicted by code 3 in Fig. 2. For example, the amplitude of the
24 pulses can be raised by the inverse of the average duty cycle. Such a technique maintains the
25 same average signal power, although other techniques can be used to boost the signal power.

26 The chip sequences during the period of high power pulses, as well as the staggered
27 time intervals between the high power pulses, are known to the receiver. For a military
28 application, the inter-pulse intervals and the specific chip sequences could be
29 cryptographically generated and therefore could be reproduced only by authorized users. As
30 depicted in Fig. 2, the receiver compares the received signal containing high power pulses
31 with the stored code 4. The comparison can be accomplished by correlating the received
32 signal with the stored code 4 by taking the dot product of the stored sequence with a

1 corresponding length of incoming signal. Then on every succeeding time sample ($\frac{1}{2}$ chip),
2 the incoming signal is shifted by one sample and a new dot product is formed. When the
3 shifted incoming signal aligns (within $\frac{1}{2}$ chip) with the stored code 4, the output of the
4 correlator, that is, the value of the dot product, will be much higher than at other times. Here,
5 unlike the conventional systems, only the chip values that are transmitted with high power
6 participate in the dot product. When the correlation process sums over the high power chips
7 and ignores the low power chips, processing gain and the resultant acquisition performance
8 (interference and jamming immunity) is improved significantly.

9 *Staggered Pulse Transmitter*

10 A spread-spectrum communications transmitter 5, such as a transmitter that can be
11 employed in a GPS satellite, is shown in Fig. 3A, configured to produce high power pulses by
12 boosting certain chips in a sequence of chips generated according to a pseudonoise (PN)
13 code. The transmitter of Fig. 3A includes a PN code generator 6 that is controlled by timing
14 counters 7 and both are driven based on a clock oscillator 8. The PN code generator 6
15 outputs a sequence of chips according to a PN code that the generator is configured to
16 generate. An amplifier 9 boosts the power level of certain chips in the sequence output from
17 the PN code generator 6. A cryptographic unit 10 controls the time interval over which the
18 amplifier operates to boost chips in the PN sequence. The cryptographic unit, using a
19 predetermined cryptographic algorithm and cryptographic keys stored in cryptographic
20 storage unit 11, determines the length of an interval of time between a group of boosted
21 chips. According to the cryptographic algorithm and keys used by the cryptographic unit 10,
22 the cryptographic unit 10 controls the amplifier to boost the power level of the PN code chips
23 above a nominal transmission value for a period of time. After that period of time elapses the
24 cryptographic unit 10 controls the amplifier so that it does not boost the power level for
25 another period of time. The cryptographic unit 10 can determine, based on the cryptographic
26 algorithm and keys in use, the time intervals over which the chips are to be boosted, not
27 boosted.

28 The output of amplifier 9 is a sequence of PN code chips having groups of sequential
29 chips with a high power level separated by groups of chips with a low power level. For
30 example, Fig. 2 shows an example PN code sequence output from amplifier 9. Here, a first
31 group of PN code chips, numbered 1 through 4, are not boosted. This first group of chips
32 corresponds to an interval of time in which the cryptographic unit 10 controls the amplifier 9

1 to not boost the power level of the chips. A second group of chips, corresponding to an
2 interval of time in which the cryptographic unit 10 controls the amplifier 9 to boost the power
3 level of the PN code chips, is shown by chip numbers 5 through 10. PN code chips numbered
4 11 through 24 span a third interval of non-boosted chips. A fourth interval includes boosted
5 chips 25 through 30, and a fifth interval includes non-boosted chips 31 through 35. As can
6 been seen in Fig. 2 the intervals of time for the groups of non-boosted chips vary in length.
7 The variations in length follow a cryptographic pattern according to the cryptographic
8 algorithm and keys in use by the cryptographic unit 10.

9 Returning to Fig. 3A, the boosted and non-boosted PN code chips output from
10 amplifier 9 are modulated with a carrier signal via modulator 13 which is driven by carrier
11 oscillator 14. Alternatively, the amplifier 9 can be configured, as shown in Fig. 3B, to
12 receive the output of the modulator 13 and amplify the modulated signal. In this instance the
13 modulator 13 operates on a fixed signal amplitude.

14 Optionally, data can be superimposed onto the code and carrier by using a modulo 2
15 adder 12 that adds data to the signal output from PN code generator 6. The transmitter 5
16 transmits the modulated carrier via antenna 15 thereby outputting a carrier wave modulated to
17 carry the boosted and non-boosted PN code chips. That transmitted signal is intelligible to a
18 receiver that has a computer-controlled correlator for detecting the sequences of high-power
19 PN code chips based on the intervals between the groups of high power chips that follow a
20 cryptographical pattern.

21 *Staggered Pulse Receiver*

22 Note that Fig. 2 shows a functional description of the process of acquiring a staggered
23 pulse signal. It will be appreciated that an ordinarily skilled artisan would understand that
24 there are many efficient ways to implement receiver to acquire such a staggered pulse signal.

25 A typical receiver has an acquisition mode that enables it to discover the correct
26 signal timing, and a tracking mode that enables it to follow any drift of the timing. Both
27 modes use mostly the same resources of the receiver, except for the correlators. The tracking
28 mode typically needs only a few correlators (generally with on-time, early, and late phases).
29 However, the acquisition mode typically needs as many parallel correlators as can be
30 afforded, to allow searching for the correct timing as quickly as possible.

1 An example of a receiver configured to operate in the tracking mode is shown in Fig.
2 4A. Here, a receiver 16 receives the transmitted signal via an antenna 17 that provides the
3 received signal to a gain controller 18, such as an amplifier. The gain controller 18 is
4 controlled by a cryptographic unit 19 that is connected to a cryptographic storage unit 20
5 for storing cryptographic keys. The cryptographic unit 19 and cryptographic storage
6 unit 20 correspond to the cryptographic unit 10 and cryptographic storage unit 11,
7 respectively, of the transmitter. The output of the gain controller 18 is applied to a
8 demodulator 21 that is driven by a carrier oscillator 22, and produces two signals out-of-
9 phase by 90° that are provided to a group of parallel correlators 23. Those two signals are
10 designated as in-phase (I) and quadrature (Q) signals. The parallel correlators can include as
11 many or as few correlators as required to track the incoming signal. Multiple parallel
12 correlators 20 can be used to correlate multiple phases of the signals, such as the early and
13 late phases of the signal.

14 The parallel correlators 23 are provided with PN reference codes that correspond to
15 the PN codes generated in the transmitter. PN code generator 24 generates the reference
16 codes. The reference codes can be delayed to correspond to the various phases to be tested.
17 Alternatively, the input signals, here the I and Q signals, can be delayed with various delays
18 and correlated with a single PN code to test the different phases.

19 The PN code generator 24 is driven by a local clock oscillator 25 and timing counters
20 26 which can produce the different timings for the PN reference codes. The local clock
21 oscillator also drives timing counters 26. The clock oscillator 25 is controlled by an output of
22 a timing adjustment unit 27 that generates a timing adjustment signal based on the output of
23 the correlators 23. For example, the difference of the strength of the early and late correlators
24 can be used to adjust the timing, assuming that the timing error is small.

25 In the receiver shown in Fig. 4A the cryptographic unit 19 generates a sequence
26 based on an algorithm and a key from the cryptographic storage unit 20 that correspond to the
27 algorithm and key used by the transmitter 5 for use in decoding the sequence of pulses. The
28 tracking mode operation is performed as in a conventional tracking receiver although with a
29 cryptographically controlled gain added as shown in Fig. 4A. It is noted that the time tracking
30 loop is shown in Fig. 4A, but not the carrier tracking loop. The cryptographic unit 19 can
31 also provide inputs to the PN code generator 24 if needed.

1 Since the tracking mode can only handle small timing errors, the receiver must first
2 use the acquisition mode to acquire correct timing. A receiver configured to operate in an
3 acquisition mode is shown in Fig. 4B. Here, many of the same components used for the
4 tracking mode are shown for use in the acquisition mode. However, when operating in an
5 acquisition mode many parallel correlators are used to try many possible timings at the same
6 time. The timing counters are not set correctly, but simply define an initial reference for
7 identifying all of the timing possibilities. Generally one (perhaps two) of the correlators will
8 have nearly correct timing, recognized by having the strongest output(s). When the correct
9 timing is confirmed, the timing counters are set correctly for the tracking mode.

10 In the acquisition mode, the correlation is performed in two stages. In the first stage,
11 performed by a parallel correlator unit 28, shown in Fig. 4B, that has many correlators for use
12 in acquiring the signal, the signal is correlated over a span of individual power pulses. In the
13 second stage, performed by a matched filter 29, these short correlations are summed, using
14 delays that match the random intervals between the power pulses. In Fig. 4B a cryptographic
15 unit 31, using keys stored in a cryptographic storage unit 32, is connected to the matched
16 filter 29 and is used to set these delays, using the same random values used in the transmitter.
17 The cryptographic unit 31 also can provide inputs to the PN code generator 24 if needed.

18 *Acquisition Strategy*

19 Suppose the receiver's initial time uncertainty is no more than plus or minus 10
20 seconds. The receiver's acquisition strategy begins by using the same pulse timing as for the
21 transmitter. Given the current time of day plus 10 seconds, the pulse timing, which can be
22 represented as a list of pulse start times, covering a correlation span is generated. The
23 correlation span is the portion of the signal that the receiver will seek to detect. In a similar
24 fashion, the PN subsequences of the code during the pulse intervals indicated by the list of
25 pulse start times is also generated. This data is used to configure the correlator circuits,
26 described below in more detail, preparing it to detect this portion of the signal, which
27 according to the receiver's timing, is 10 seconds in the future.

28 If the receiver's timing error is 10 seconds late, then the correlator will detect the
29 signal immediately (looking early compensates for its lateness); but if set 10 seconds early,
30 will detect it after searching for 20 seconds. For all errors within the uncertainty range, the
31 signal will be found sometime in the 20-second search.

Correlator Structure

The correlator used to detect a portion of the code repeatedly computes dot products, each one being a dot product of a subsequence of recent signal samples and a subsequence of the code to be detected. The dot product (correlation) becomes large when the two subsequences align and match well. Two types of correlators that can be used in the parallel correlators 23 use different methods of alignment. A matched-filter type of correlator is shown in Fig. 5A and a parallel-active type of correlator is shown in Fig. 5B.

The matched filter type of correlator shown in Fig. 5A includes a code register 33a that receives a reference code and performs an off-line shift, a signal register 33b that receives the received signal and performs a real-time shift, and a dot product unit 34 that performs a dot product operation on its inputs. The contents of the code and signal registers are input to the dot product unit that performs the dot product operation on the inputs and outputs a correlation result.

As shown in Fig. 5B, the parallel-active type of correlator shown in Fig. 5B includes flip-flops 35a and 35b, multipliers 36a through 36d, a register 37, adders 38a through 38d, and registers 39a through 39d that are dumped to produce correlation outputs corresponding to different times (e.g., time $t=0$, $t=1$, etc.). Each output circuit includes a register (e.g., register 39a) receiving an input from an adder (e.g., 38a) that adds the output of the register with an output of a multiplier (e.g., multiplier 36a). When the register dumps a "0" is inserted into the adder (e.g., 38a) at the appropriate time to, in essence, reset the accumulation. The multiplier multiplies a received signal at the sample rate with a reference code at the chip rate. The flip-flops delay the reference code or the received signal for an appropriate amount of time for the corresponding correlation result. A multiplexer (not shown) can be used to multiplex the values dumped from the registers at different times.

Detecting a Pulse

To coherently detect one pulse, either type of correlator can be used equal in size to the width of the pulse. For example, to detect one pulse in the staggered pulse signal using the matched filter type correlator the correlator's code register 33a holds as many chips as in the pulse, and signal register 33b holds as many samples as in the pulse. To detect one pulse in the staggered pulse signal using the parallel-active type correlator the correlator's code register (i.e., flip-flops 35a, 35b, etc.) holds as many chips as in the pulse. However, the

1 signal register (i.e., register 37) holds as many samples as in a chip, as opposed to the number
2 of samples in a pulse as in the matched-filter type of correlator. For the parallel-active style
3 correlator, the code register should be rotated after it is initially filled, and each sum dumped
4 and reset after it receives the last chip. In this way, both styles can search for a given pulse
5 for a time equal to the span of the time uncertainty.

6 *Detecting Multiple Code Pulses*

7 To coherently detect multiple randomly spaced pulses, either type of correlator can be
8 used, with the receiver configured with one correlator for each pulse. To noncoherently sum
9 the individual pulse correlations into one stronger correlation, these correlators are strung
10 together with variable-delay memories that are configured with delays matching the random
11 intervals between the pulses. Here, more differences between the correlator styles are noted.

12 When using the matched-filter correlators, advantage is taken of the fact that the
13 signal register of each pulse-detection correlator delays the signal for the width of the pulse.
14 Variable delays set to the intervals between pulses are used, as illustrated in Figs. 6A and 6B.
15 Fig. 6A shows a receiver configured with matched-filter correlators for detecting a pulsed
16 code. In Fig. 6A matched-filter correlators 40a through 40d are connected with delay units
17 42a through 42d disposed between the correlators. For a noncoherent sum of the pulse
18 correlations, the vector outputs of the correlators are squared (to compute $I^2 + Q^2$) by
19 squaring units 41a through 41b that square the correlation outputs. The squared correlation
20 outputs are summed using an adder 43 to produce a detection signal. Only the signal path is
21 shown in Fig. 6A.

22 However, when using the parallel-active type correlators, the signal registers do not
23 have any substantial delay. Each variable delay is set to the interval from the start of one
24 pulse to the start of the next pulse, as shown in Fig. 6B. In Fig. 6B variable delay units 44a
25 through 44c receive the signal and delay it according to their set delay values. Parallel-active
26 type correlators 45c through 45d receive the delayed signal, corresponding the corresponding
27 interval between pulses, and produce a correlation result that can be squared by square units
28 46a through 46d. The squared correlation results are summed by an adder 47 to produce a
29 detection signal.

1 It will also be understood that many of the elements shown in the transmitter
2 illustrated in Figs. 3A-B and the receiver illustrated in Figs. 4A-B can be implemented in
3 hardware, software or firmware.

4 *Applications*

5 A staggered pulse acquisition system is applicable for significantly improving A/J for
6 the military code for the next generation of GPS. It is also generally applicable for improving
7 interference immunity, in general, for spread spectrum communications and radar systems.

8 Having described embodiments of a staggered pulse signal, and methods and
9 apparatuses for transmitting and receiving such a signal, it is believed that other
10 modifications, variations and changes will be suggested to those skilled in the art in view of
11 the teachings set forth herein. It is therefore to be understood that all such variations,
12 modifications and changes are believed to fall within the scope of the present invention as
13 defined by the appended claims. Although specific terms are employed herein, they are used
14 in their ordinary and accustomed manner only, unless expressly defined differently herein,
15 and not for purposes of limitation.